IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION OF

LITAIZE et al.

Group Art Unit: Unassigned

Appln. No.: Unassigned

Examiner: Unassigned

Filed: Even date herewith

Atty Dkt: 81674-307205
C# M#

Title: ***MEMORY COMPONENT WITH MULTIPLE TRANSFER FORMATS***

* * * * *

INFORMATION DISCLOSURE STATEMENT

Attached is Form PTO-1449 listing references to be made of record. Copies of the references are enclosed.

This IDS is intended to be in full compliance with the rules, but should the Examiner find any part of its required content to have been omitted, prompt notice to that effect is earnestly solicited, along with additional time under Rule 97(f), to enable Applicant to comply fully.

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed Form PTO-1449 with the Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Dated: December 18, 2003

Respectfully submitted,
Pillsbury Winthrop LLP

By: /Roger R. Wise/
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FORM PTO-1449 (Modified) **LIST OF PATENTS AND PUBLICATIONS FOR INFORMATION DISCLOSURE STATEMENT BY APPLICANT(S)** (Use several sheets if necessary)	Docket Number: 81674-0307205	Serial Number:
	Applicant(s): Litaize et al.	
	Filing Date:	Group:

U.S. PATENT DOCUMENTS

Examiner Initial *	ID	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	AA	5 2 8 7 5 3 2	2/15/94	Hunt			
	AB	5 1 5 7 7 7 6	10/20/92	Foster			
	AC	5 0 2 3 8 3 8	6/11/91	Herbert			
	AD	4 9 6 1 1 7 1	10/2/90	Pinkham et al			
	AE	4 9 3 0 0 6 5	5/22/90	McLagan et al			
	AF	4 7 8 2 4 3 9	11/1/88	Borkar et al			
	AG	4 7 4 7 0 8 1	5/24/88	Heilveil et al			
	AH	4 7 0 4 6 7 8	11/3/87	May			
	AI	4 6 4 4 4 6 9	2/17/87	Sumi			
	AJ	4 6 4 1 2 7 6	2/3/87	Dunki-Jacobs			
	AK	4 6 3 9 8 9 0	1/27/87	Heilveil et al			
	AL	4 4 6 8 7 3 3	8/28/84	Oka et al			
	AM	4 4 2 6 6 8 5	1/17/84	Lorentzen			
	AN	4 4 0 8 2 7 2	10/4/83	Walters			
	AO	4 2 5 7 0 9 7	3/17/81	Moran			
	AP	3 8 4 6 7 6 3	11/5/74	Riikonen			
	AQ	H 6 9 6	10/3/89	Davidson			

OTHER ART (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	CA	Hopper et al., *Multiple vs. Wide Shared Bus Multiprocessors*, Proceedings of the 16th Annual International Symposium on Computer Architecture, Jerusalem, Israel, June 1989, IEEE Computer Society Press, 1989.
	CB	International Search Report, Application No, PCT/FR 88/00608, Date of Mailing of the International Search Report, 29 March 1989 (29.03.89).
	CC	Gehringer et al., *A Survey of Commercial Parallel Processors*, Computer Architecture News, Vol. 16, No. 4, Sept. 1988.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformanc and not consid red. Includ copy of this f rm with next communication to applicant.

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FOREIGN PATENT DOCUMENTS

	ID	DOCUMENT NUMBER			DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
									YES	NO
	BA	JP	120553/1987		6/1/1987	Mitsuse, Masakazu			X	
	BB	EP	0 189 576	A2,A3	8/6/1986	Texas Instruments Inc.				
	BC	EP	0 187 289	A2,A3	7/16/1986	IBM				
	BD	EP	0 166 192	A2,A3	1/2/1986	IBM				
	BE	EP	0 126 976	A2	12/5/1984	IBM				
	BF	JP	135684/1984		8/3/1984	Nojima, Kenichi			X	
	BG	WO	82/02615	A1	8/5/1982	Western Electric Company				
	BH	JP	33471/1982		2/23/1982	Kadota, Haruhiko			X	

OTHER ART (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	CD	French Search Report, Application No. FR 87181003 (FR19870018103 19871214), Date of Completion: August 8, 1988.

	CE	Hwang et al., *Computer Architecture and Parallel Processing*, Chapter 9, McGraw-Hill, 1984.

	CF	Dubois et al., *Effects of Cache Coherency in Multiprocessors*, IEEE Transaction in Computers, Vol. C31, No. 11, pgs. 1083-1099,
		November 1982.

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	AR	5	8	4	7	9	9	7	12/8/98	Harada et al.			
	AS	5	3	9	0	1	4	9	2/14/95	Vogley et al.			
	AT	5	3	6	1	2	7	7	11/1/94	Grover			
	AU	5	3	0	1	2	7	8	4/5/94	Bowater et al.			
	AV	5	2	0	6	8	3	3	4/27/93	Lee			
	AW	5	1	4	8	5	2	3	9/15/92	Harlin et al.			
	AX	5	1	4	2	6	3	7	8/25/92	Harlin et al.			
	AY	5	1	4	0	6	8	8	8/18/92	White et al.			
	AZ	5	1	0	9	4	9	8	4/28/92	Kamiya et al.			
	DA	5	1	0	7	4	6	5	4/21/92	Fung et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER			DATE	Name of Patentee or Applicant of Cited Document			TRANSLATION	
									YES	NO
	BI	JP	61028248	A2	2/7/86	Yamashita Atsus et al.				
	BJ	JP	58184647	A2	10/28/83	Ibuki Yaschiko				

OTHER ART (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	CG	T. Williams et al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, Vol. 23, No. 5, pp. 1085-1094, Oct. 1988
	CH	D.T. Wong et al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5-μm Devices", IEEE Journal of Solid State Circuits, Vol. 23, N . 5, pp. 1095-1103, Oct. 1988
	CI	D. Jones, "Synchronous Static RAM", Electronic and Wireless World, Vol. 93, No. 1622, pp. 1243-1244, (plus 2 sheets of the Journal's Cover and Table of Contents), Dec. 1987
	CJ	F. Miller et al., "High Frequency System Operation Using Synchronous SRAMS", Midcon/87 Conference, pp. 430-432, Chicago, IL: USA, Sep 15-17, 1987

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	DB	5	0	8	3	2	9	6	1/21/92	Hara et al.			
	DC	5	0	7	7	6	9	3	12/31/91	Hardee et al.			
	DD	5	0	1	8	1	1	1	5/21/91	Madland			
	DE	5	0	1	6	2	2	6	5/14/91	Hiwada et al.			
	DF	4	9	7	5	8	7	2	12/4/90	Zaiki			
	DG	4	9	7	0	4	1	8	11/13/90	Masterson			
	DH	4	9	5	4	9	8	7	9/4/90	Auvinen et al.			
	DI	4	9	5	3	1	2	8	8/28/90	Kawai et al.			
	DJ	4	9	5	1	2	5	1	8/21/90	Yamaguchi et al.			
	DK	4	9	3	7	7	3	4	6/26/90	Bechtolsheim			

OTHER ART (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	CK	S. Muchmore, "Designing Computer Systems Based on Multibus II", New Electronics, Vol. 20, No. 16, p. 31-32, Aug. 11, 1987

	CL	T.C. Poon et al., "A CMOS DRAM-Controller Chip Implementation", IEEE Journal of Solid State Circuits, Vol. 22, No. 3,
		pp. 491-494, Jun. 1987
	CM	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, Vol. 21, No. 5, pp. 649-654,
		Oct. 1986
	CN	"Accordion Start-Stop Sequencer for a Variable Cycle Storage Controller", IBM Technical Disclosure Bulletin, pp. 2074-2075,
		(a delphion.com reprint on two sheets), Oct. 1986
	CO	"Motorola 68030 Cache Organization", posting to Internet Newsgroup net.arch by aglew@ccvaxa.UUCP,
		(a google.com reprint on two sheets), Sep. 29, 1986
	CP	Raymond Pinkham et al., "A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video
		Applications", IEEE Journal of Solid State Circuits, Vol. SC-19, No. 6, pp. 999-1007, Dec. 1984
	CQ	L.R. Metzeger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, Vol. 18, No. 5,
		pp. 562-567, Oct. 1983

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	DL	4	9	2	8	2	6	5	5/22/90	Higuchi et al.			
	DM	4	9	2	0	4	8	3	4/24/90	Pogue et al.			
	DN	4	9	1	6	6	7	0	4/10/90	Suzuki et al.			
	DO	4	9	1	2	6	3	0	3/27/90	Cochcroft, Jr.			
	DP	4	8	8	2	7	1	2	11/21/89	Ohno et al.			
	DQ	4	8	4	5	6	6	4	7/4/89	Aichelmann, Jr. et al.			
	DR	4	8	2	1	2	2	6	4/11/89	Christopher et al.			
	DS	4	8	0	7	1	8	9	2/21/89	Pinkham et al.			
	DT	4	7	9	9	1	9	9	1/17/89	Scales, III et al.			
	DU	4	7	8	8	6	6	7	11/29/88	Nakano et al.			

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	CR	M. Bazes et al., "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking And Correction", IEEE Journal of Solid State Circuits, Vol. 18, No. 2, pp. 164-172, Apr. 1983
	CS	T.L. Jeremiah et al., "Synchronous LSSD Packet Switching Memory and I/O Channel", IBM Technical Disclosure Bulletin, Vol. 24, No. 10, pp. 4986-4987, (a delphion.com reprint on a single sheet), Mar. 1982
	CT	R.W. Callahan et al., "Burst-Mode PIO Bus Control", IBM Technical Disclosure Bulletin, Vol. 21, No. 4, pp. 1417-1419, (a delphion.com reprint on two sheets), Sep. 1978
	CU	Stanley D. Rosenbaum et al., "A 16 384-Bit High-Density CCD Memory", IEEE Journal of Solid State Circuits, Vol. SC-11, No. 1, pp. 33-39, Feb. 1976

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	DV	4	7	3	4	8	8	0	3/29/88	Collins			
	DW	4	6	8	0	7	3	8	7/14/87	Tam			
	DX	4	6	7	5	8	5	0	6/23/87	Kumanoya et al.			
	DY	4	5	7	0	2	2	0	2/11/86	Tetrick et al.			
	DZ	4	5	1	9	0	3	4	5/21/85	Smith et al.			
	EA	4	4	4	5	2	0	4	4/24/84	Nishiguchi			
	EB	4	3	1	5	3	0	8	2/9/82	Jackson			
	EC	4	2	4	7	8	1	7	1/27/81	Heller			
	ED	4	1	8	3	0	9	5	1/8/90	Ward			
	EE	4	0	9	2	6	6	5	5/30/78	Saran			
	EF	4	0	8	4	1	5	4	4/11/78	Panigraphi			
	EG	3	8	2	1	7	1	5	6/28/74	Hoff, Jr. et al.			

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